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Simulation of High-K Dielectric Gate Effect on Carrier Mobility Using SILVACO TCAD

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Abstract—*Fabrication of MOSFET is easier than that of BJT and it consumes less power in operation. To follow the MOORE's law we have come to a conclusion to adopt the high–k dielectric gate concept but the consequence of using high–k dielectric created certain adverse effects on the working of devices. In this paper we are describing the mobility related issue. The degradation of mobility because of Coulomb scattering, Phonon scattering and other methods have been concentrated upon. The improvement aspects for mobility degradation have also been focused .This paper gives detail about the mobility in these devices with SiO2 and other high-k dielectric materials (Hfo2) .*

Keywords*: mobility; Phonon scattering; Carrier trapping; Coulomb scattering;*

1. INTRODUCTION

Over the past three decades, CMOS technology scaling has been a main factor of the electronics industry. It has provided a way towards both denser and faster integration process. The transistors manufactured today are 20 times faster and takes less than 1% of the area of those built three decade before. The number of transistors per chip and the system performance has been excelling exponentially over the last two decades according to Moore's law. As the channel length is reduced, the performance improves, the power per switching event decreases, and the density improves. But the power density, total circuits per chip, and the total chip power consumption has been increasing.The requirement for more performance enhancement and integration has boosted the scaling trends in almost every device parameter, such as effective device leakage, channel length, supply voltage gate dielectric thickness, etc. SiO2 has been used as a gate oxide material for decades.

As the thickness scales down 2nm, leakage currents due to tunneling increase exponentially, leading to high power consumption and reduced device reliability. Replacing the SiO2 gate dielectric with a high-K ma terial allows increased without the short channel Effects. It

Effects. Since it Effects. Since it becomes very much necessary to replace the SiO2 with a thicker layer of oxides of higher dielectric constant (K), there are many oxides for option for this purpose such as HfO2, hafnium silicate, ZrO2 and various lanthanides and it was realise that in many ways they have inferior electronic properties than SiO2, such as a tendency to crystallize and a high concentration of electronic defects. The purpose of using high-k oxides in place of SiO2 is to create denser and faster devices. The speed of the device follows source to drain current, which depends on the carrier mobility. The effective mobility is defined in terms of the drain current, in the linear region as:

$$ID=\mu nWL\{(VGS-Vth)VDS-VDS22\} \quad \ldots. (I)$$

One of the major issues with high-k/metal gate is degradation of effective mobility. CMOS devices with SiO2 gate oxide has mobility around to 300 cm/V-s for the electric field and doping concentration used. The mobility provided by high K oxides is below this value. It is easily expected that effective mobility is reduced by high-k directly in contact of Si as shown in figure 1. The mobility is limited due to interface roughness of surface over the range.

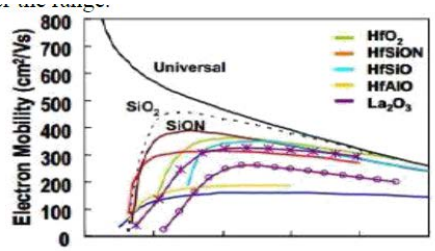

Fig 1: Degradation in Effective Mobility Using High-K Gate Oxides As Compared To SiO2

2. MOBILITY DEGRADATION

Mobility degradation is one of the major drawbacks of using high–K materials as a gate oxide as an Alternative to SiO2 in Metal Oxide semiconductor field effect transistors (MOSFET). There are certain mechanisms of decrease in mobility of the charge carriers. These details to the internal mechanisms of the device which has to be investigating carefully and can be stated only after careful observation.

There are certain remedies which can fix the drawback of decrease in mobility, which are discussed at the end of this paper. The observations made by Zhu [2] suggested that the mobility of electrons and holes depends only on the effective gate field and Si surface [5]. The individual components of mobility add according to Matthiessen's rule,

$$1\mu = 1\mu c + 1\mu FN + 1\mu SR \qquad (ii)$$

μC Is the mobility of the columbic scattering

μPS Is the mobility of phonon scattering

μSR Is the mobility of surface roughness

The mobility is decreased by different factors at different electric fields, as each obeys a different power law with field. At low fields, mobility is limited by Columbic scattering(*C*) by trapped charges in the oxide, channels and gate electron interface; at moderate field it is limited by phonon scattering (*PH*), and at high fields by scattering by surface.

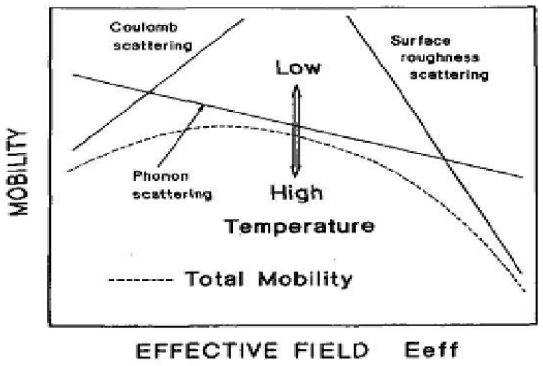

Fig. 2: Schematic carrier mobility vs. vertical field in FETs in the universal mobility model

Coulomb scattering

The coulomb scattering due to interface trapped charge is the dominant mechanism of mobility degradation of high k gated MOSFETS at low fields. There is reason because the fact that the energy distribution of the of the interface traps is observed to be asymmetric as shown in figure 3

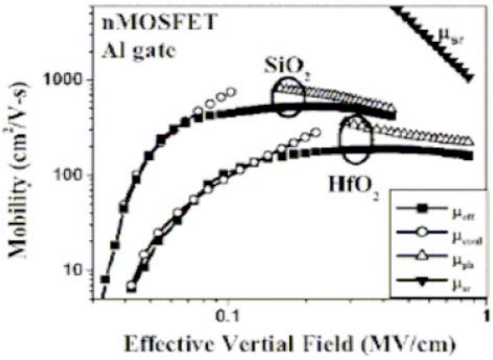

Fig. 3: Effective mobility for the two samples, HfO2 and SiO2 samples due to Coulomb scattering and Phonon scattering

The interface trap density near the conduction band edge is higher than that near the valence edge as observed by the larger sub-threshold swing of the n-MOSFET as compared to that of the p-MOSFET. Hence, the decrease of hole mobility in p-MOSFET is generally less fatal than that for electron mobility in n-MOSFET as shown in fig. Coulomb scattering is mainly due to the electrostatic forces on the electrons when electric field is present.

B. Phonon scattering

In addition to Coulomb scattering caused by high densities of interface traps and oxide charge, the scattering due to soft optical phonons is a fascinating possibility that can't be denied and the possibility is captured in figure. As shown in figure the mobility limited by phonon scattering in HfO2 gated MOSFETS is lower than SiO2 gate oxides. MOSFETS with quite high-k oxides such as HfO2 has an additional source of phonon scattering.

3. SIMULATIONS RESULTS

In this paper we take reference of the paper by Zhu, W. and Ma, T., "Temperature Dependence of Channel Mobility in HfO2-Gated NMOSFETs".We implemented high –k dielectric gate effect on mobility of carries using Silvaco ATLAS tool by theoretical observations we implemented mobility variation model due to high-k dielectric using TCAD.

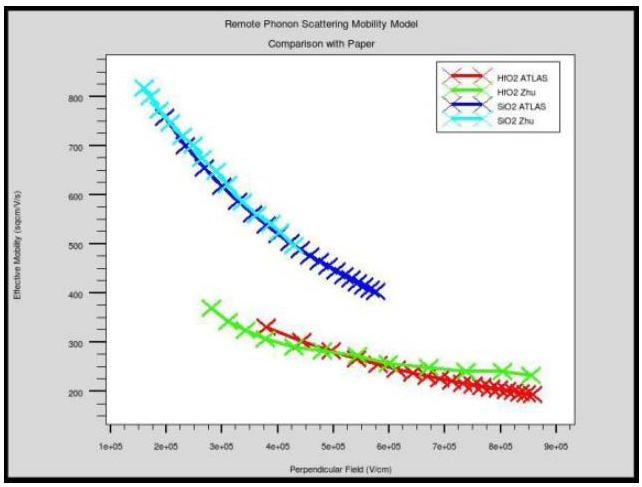

Fig. 4: Phonon Scaterring model using silvaco Atlas

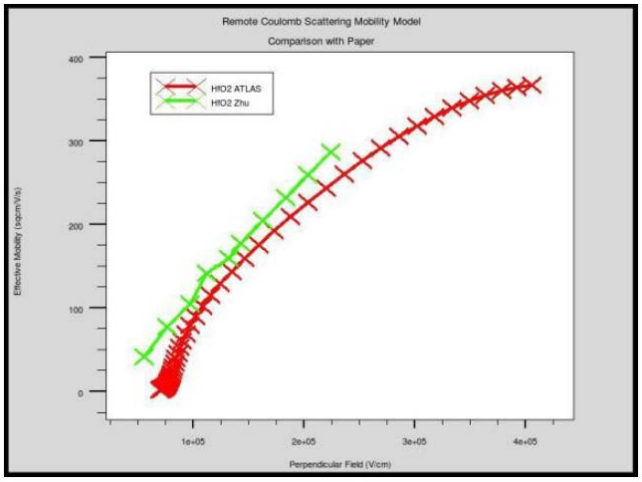

Fig. 5: Remote Colomb scaterring Model Using silvaco Atlas

4. METHODS TO IMPROVE MOBILITY

The problem of mobility degradation can be resolved by replacing the poly-silicon gate electrode with metal gate . The conductivity of the poly-silicon layer is very low and due to this low conductivity, the charge accumulation is low, leading to a delay in channel formation and thus unwanted delays in circuits. The poly layer is doped with N-type or P-type impurity to make it behave like a perfect conductor and reduce the delay. Doped poly-silicon is a semiconductor, and thus will form a "depletion" region when voltage is applied.

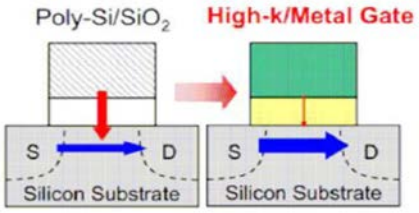

Fig 6: Replacement of Poly-Si/SiO2 with high-k/metal Gate

This "depletion region" behave very much like a thicker oxide, in that it lowers inversion charge (thus reducing capacitance of inversion layer)with resulting decrement in drive current. The metal gate consists free carrier density more than 1×1020/cm3, which helps for it possible to dynamically screen the longitudinal soft optical phonon modes arising from high-K dielectric materials. The metal gate electrodes assist to screen the dipole coupling of remote phonon scattering. Thus are able to reduce phonon scattering and reduce the mobility degradation problem

The effect of dipole vibrations on the channel electrons can be reduced significantly by increasing the density of electrons in the gate electrode. Figure 7 represents how mobility is improved by replacing poly- Si with metal gate. Thus high-K oxides with metal gate have higher mobility than with poly-Si gate

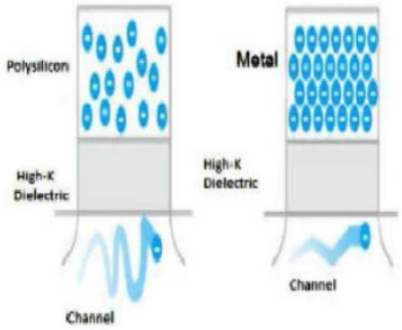

Fig. 7: Increase in channel mobility by replacing poly-silicon gate with a metal gate

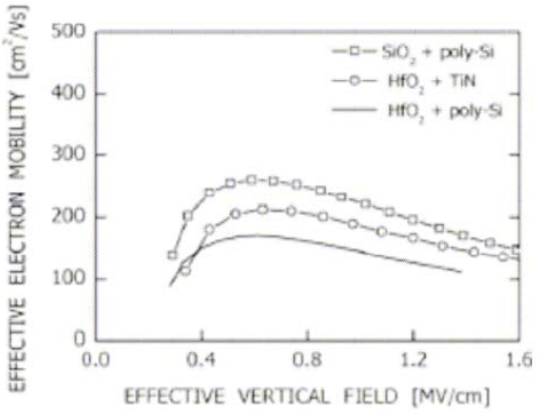

Fig. 8: Effective electron mobility for a) HFO_2 with poly-Si b) HFO_2 with TiN c) SiO_2 with Poly-Si.

5. CONCLUSION

This Paper discusses the effect of High-K oxides on the mobility of charge carriers, accurate measurements and degradation mechanisms of charge carriers with HfO2 as dielectric. The commonly encountered sources of error, like, trapping by high densities of interface traps leads to over counting of inversion charge carriers, high gate leakage current through ultra-thin high-K film could result in underestimation of mobility at high fields, the large channel resistance in weak inversion could result in high artificial mobility at low fields, error due to contact resistance for short channel MOSFETS. Certain mechanisms of mobility degradation have also been focused. Coulomb scattering due to interface traps is a major cause of mobility degradation. Soft optical phonons also contribute to mobility degradation. Remedies for the escalation in mobility values have also been discussed.

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